DATA BRICK DS-VU3P-PCIE

user's manual

02/09/2017

Design Service Division

PALTEK CORPORATION
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Revision History

The following table shows the revision history for this document.

version	Revision	Date	Updater	Remarks
0.0	New	01/23/2017	Inohara	—
1.0	Initial release	02/09/2017	Yanase	—

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1. Introduction

The DS-VU3P-PCIE is featuring a Xilinx VIRTEX® UltraScale+™ FPGA.

1.1. Board features

- VIRTEX® UltraScale+™(XCVU3P-2FFVC1517) is mounted on the PCIe Mother Board v0.7.
- Input Voltage : 12V
- Power : 0.85V, 0.9V, 1.2V, 1.5V, 1.8V, 3.3V(Linear Technology)
- Board size conforms to PCI-Express.
- SAMTEC FireFly ×4
- 16 lanes with PCI - Express 3.0.
- DDR4 Memory MT2400 8GB(with ECC)up to 16GB (without ECC,option)

2. Feature desgription

2.1. PCB information

Figure 1 shows the DS-VU3P-PCIE. Each numbered feature that is referenced in Figure 1 is described in Table 1.

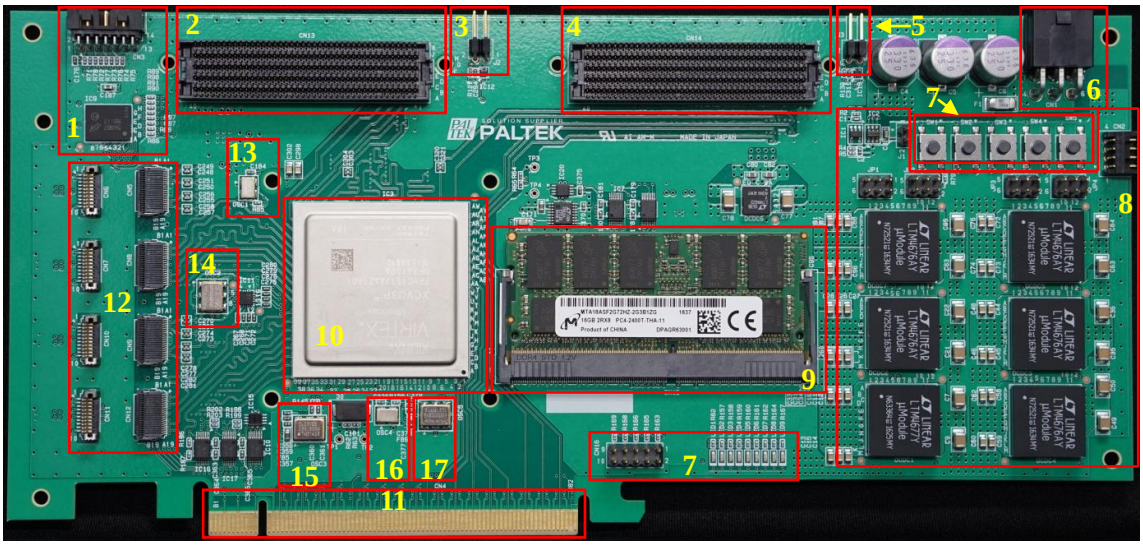

Figure 1 Product Photo

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Table 1 Board Component Descriptions

Callout	Component Description	Page Number
1	BPI Memory for Configuration and JTAG	9 (Only BPI)
2	FMC-1 HPC Connector	6
3	for FMC-1 JTAG connection	6
4	FMC-2 HPC Connector	6
5	for FMC-2 JTAG connection	6
6	6pinATX-PCIe12V IN	7
7	SW/LED/test terminal	8
8	DCDC, LT PowerPlay connector	14
9	DDR4-SODIMM	9
10	XCVU3P-2FFVC1517	10
11	PCIexpress ×16	11
12	FireFly connector	11
13	OSC1 100MHz oscillator for Configuration	12
14	OSC2 Si570 GTY Reference Clock	12
15	OSC3 200MHz Reference Clock for MIG	12
16	OSC4 100MHz oscillator for user logic	12
17	OSC5 Si570 oscillator for user logic	12

2.2. Physical Specifications

DS-VU3P-PCIE complies with PCI - Express 3.0.

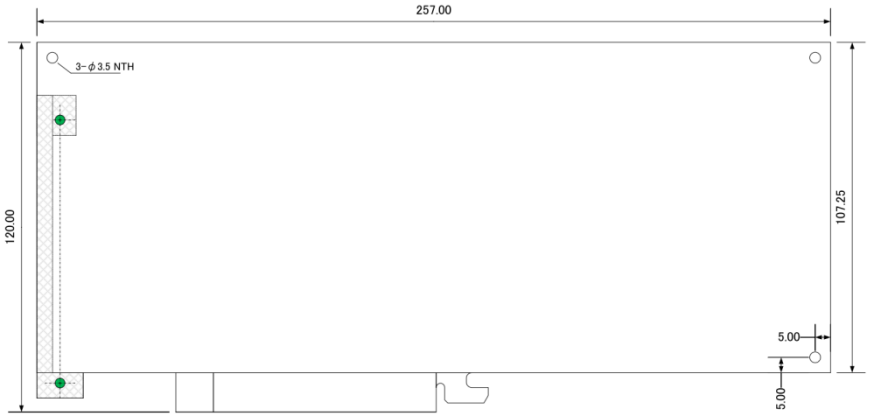

Figure 2 Mechanical Dimensions (mm)

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3. Functional Description

3.1. FMC connector

・When FMC card is implemented and PRSNT_M2C_L terminal is not connected to GND on a board, the user cannot use the TDO-TDI chain of the JTAG signal.

・JTAG of the Mezzanine side and JTAG chain of the Mother board side are constructed by short-circuiting with a jumper terminal implemented beside a connector in the case of the above.

・If the user is connecting the PRSNT_M2C_L to the GND on the mezzanine card side and the mezzanine card side where the JTAG is not used, make the TDO-TDI short on the mezzanine card side.(*Overall JTAG chain cuts.)

・FMC transceiver (GTY)ch(dp0) attaches the iBERT sample design using the loopback card (cyber Tateno).

→The above statement confirmed movement to 16Gbps.

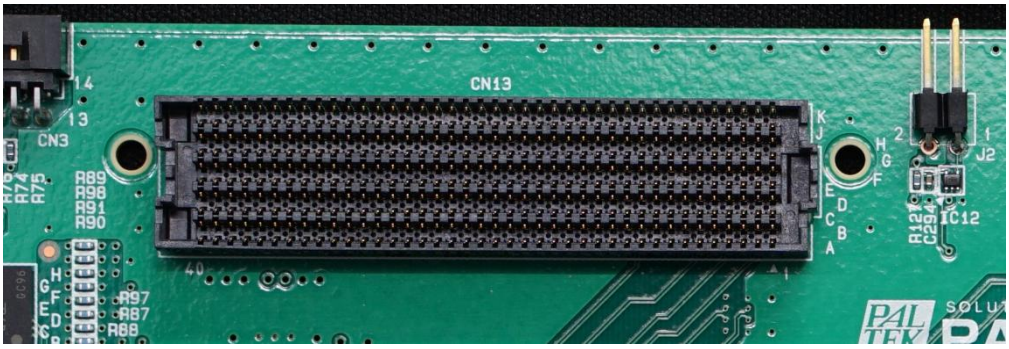

Figure 3 FMC-1 connector (CN13) and JTAG connection jumper (J2)

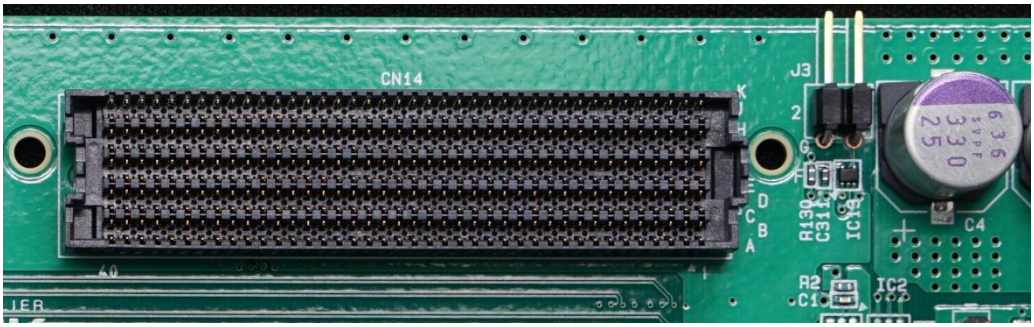

Figure 4 FMC-2 connector (CN14) and JTAG connection jumper (J3)

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3.2. Power input

The user connects 6pin connector for PCI-Express cards by ATX power supply.

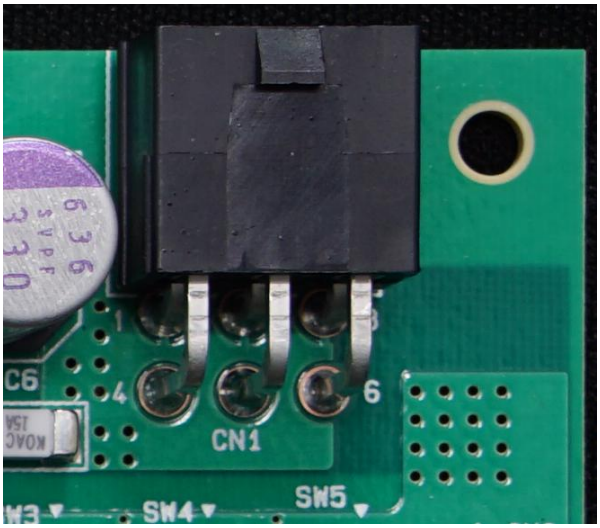

Figure 5 About ATX PCIe 6pin power supply connection connectors(CN1).

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3.3. SW/LED/test terminal

・The left switch is Re- CONFIG.

・As for the switch for user logics, it is not done PULLUP on a board. Therefore, please do PULLUP in the FPGA inside.

・It is assigned BANK47/VCCO=1.8V.

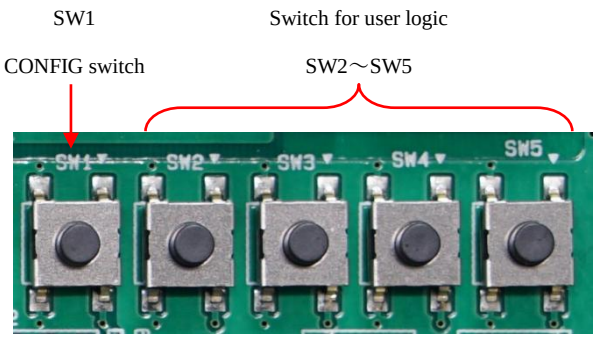

Figure 6 Switches

Table 2 Pin assignment

reference number of circuit diagram	Schematic Net Name	Pin number of FPGA terminal
SW2	PSW_0	K10
SW3	PSW_1	K11
SW4	PSW_2	L9
SW5	PSW_3	L10

・The left LED is CONFIG_DONE. When configuration of FPGA is completed, LED turn on.

・The user LED turns on with "1". (ActiveHI)

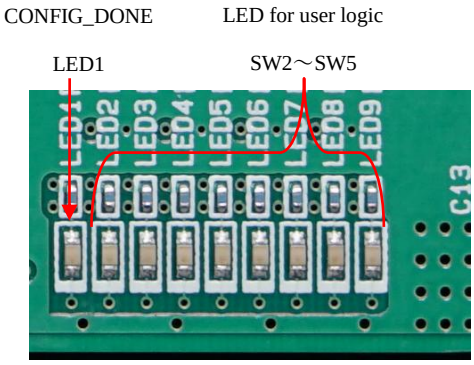

Figure 7 LEDs

Table 3 Pin assignment

reference number of circuit diagram	Schematic Net Name	Pin number of FPGA terminal
LED2	LED_0	N12
LED3	LED_1	N11
LED4	LED_2	N9
LED5	LED_3	M9
LED6	LED_4	M11
LED7	LED_5	M10
LED8	LED_6	M12
LED9	LED_7	L12

・The test terminal is connected to VCCO(Bank47) of 1.8V. It is not 3.3V interface.

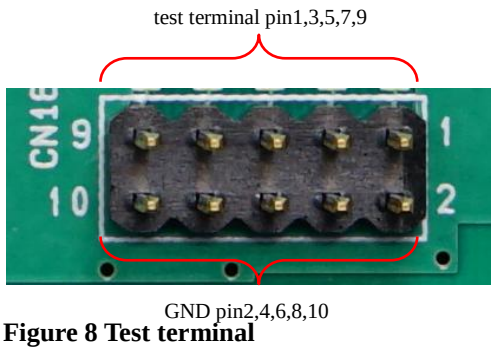

Figure 8 Test terminal

Table 4 Pin assignment

reference number of circuit diagram	Schematic Net Name	Pin number of FPGA terminal
CN16-PIN1	TP_0	H8
CN16-PIN3	TP_1	H9
CN16-PIN5	TP_2	H7
CN16-PIN7	TP_3	J8
CN16-PIN9	TP_4	N13

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3.4. DDR4-SODIMM

- Part number : MTA18ASF2G72HZ-2GB3 (Micron)
- MT-2400
- Supports 8GB(with ECC) and 16GB(w/o ECC) modules.
- Sample design (MIG-example Design) attachment using the 16G module.

  →The design which uses 16G/72bit module (MTA18ASF2G72HZ-2GB3)

3.5. BPI Flash Memory

- Part number : MT28GU01GAAA1EGC-0SIT (Micron)
- Supply voltage : 1.8V
- Data Path width : 16bit
- Device Density : 1Gb

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3.6. FPGA XCVU3P-2FFVC1517

・The device name on VIVAD is XCVU3P-FFVC1517.

・The BANK layout diagram of the FPGA used for this board and its application are shown below.

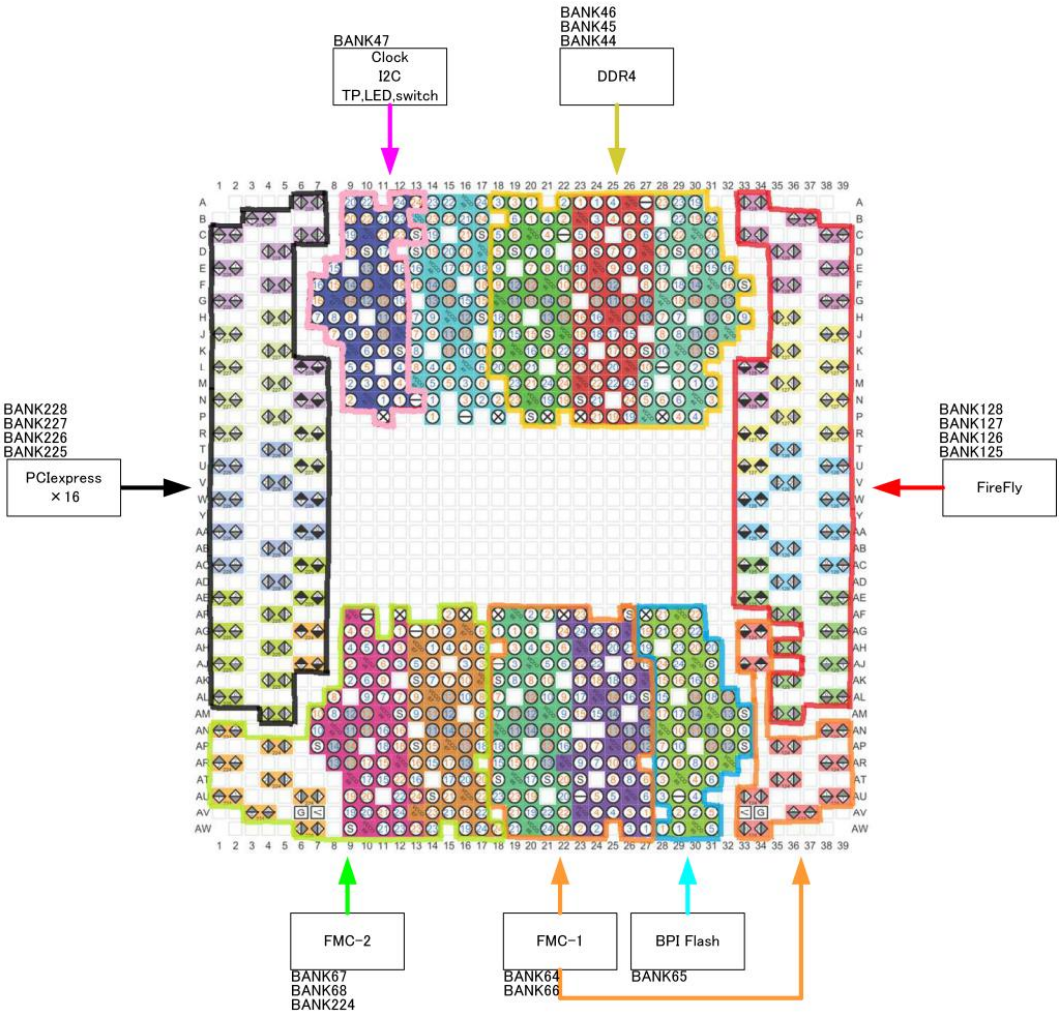

Figure 9 BANK layout diagram

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3.7. PCIexpress ×16

・Supports Gen3.

・PCIe endpoint Example-Design generated in IP catalog.

→Device drivers are not attached to the above design.

→Property check is possible on the device manager of WIN 10.

→Internal status signal can be checked on VIVADO's Hardware-Manager.

3.8. FireFly connector

・Supports ECUE (28 Gbps 300 mm) and ECUO(optical module 14 Gbps) of SAMTEC Fire-Fly connector.

・iBERT sample design combined with transceiver ch on FMC.

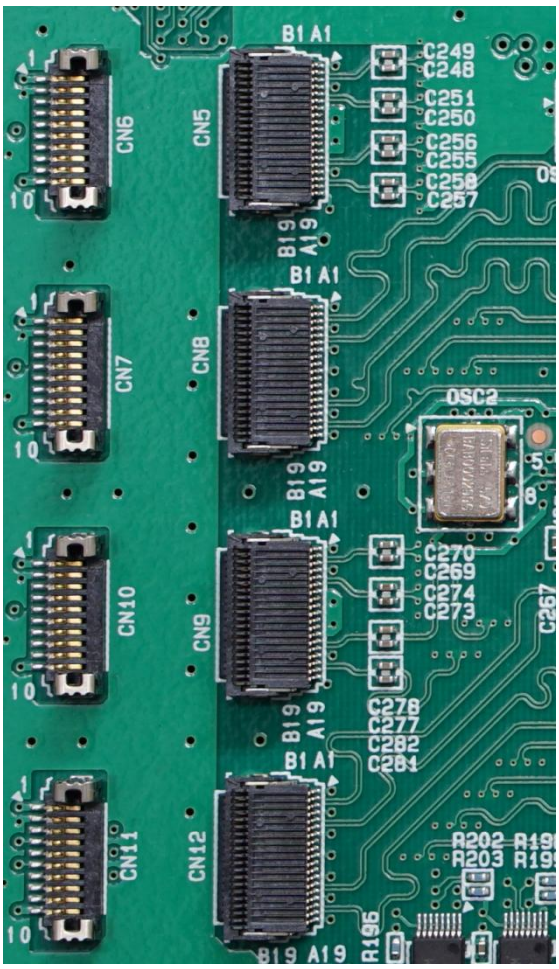
・The reference clock is connected to REFCLK 0 of each QUAD.

TX-1
Transmitter 8lane
QUAD125,126

RX-1
Receiver 8lane
QUAD125,126

TX-2
Transmitter 8lane
QUAD127,128

RX-2
Receiver 8lane
QUAD127,128



OSC2
GTY Reference Clock Si570
10-810MHz
Startupfrequency=200MHz
I2C-Address=60H

Figure 10 FireFly connector

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3.9. Oscillator

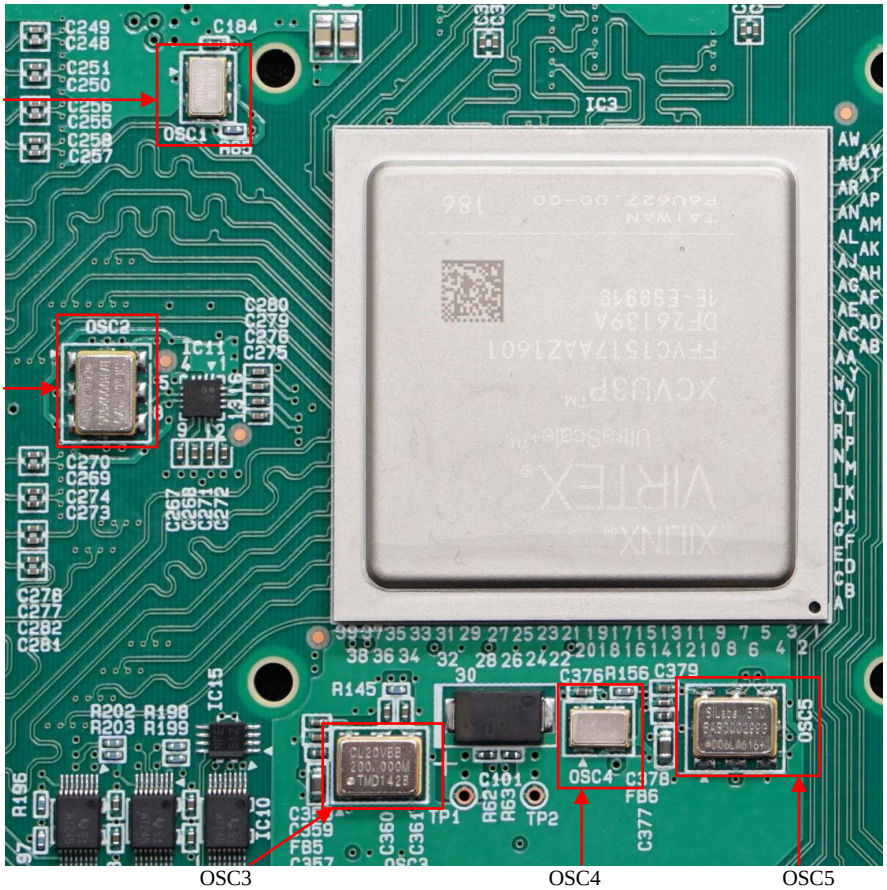
・Five oscillators are mounted on the board, and OSC 4 (fixed 100 MHz) and OSC 5 (variable Si 570) are for user logic.

Table 5 Oscillator description table

reference	IO standard	Terminal assignment	description
OSC1	CMOS	AJ28	Configuration
OSC2	LVDS	6/7(Si53340)	GTY-QUAD125-128
OSC3	DIFFSSTL12-DIC	J30/K30	200MHz for MIG
OSC4	LVCMOS18	G11	User 100MHz
OSC5	LVDS	F9/G9	DIFFTERM is necessary.

OSC1
100MHz EMC Clock for configuration

OSC2
Si570 reference Clock for GTY-QUAD125-128



OSC3
200MHz fixation reference Clock for MIG(DDR4)

OSC4
100MHz fixation Clock for user logic

OSC5
Si570 Variable Clock for user logic

10-810MHz
Startupfrequency=200MHz
I2C-Address=60H

Figure 11 Oscillators

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3.10. Clock system diagram

The clock system diagram of this board is shown below.

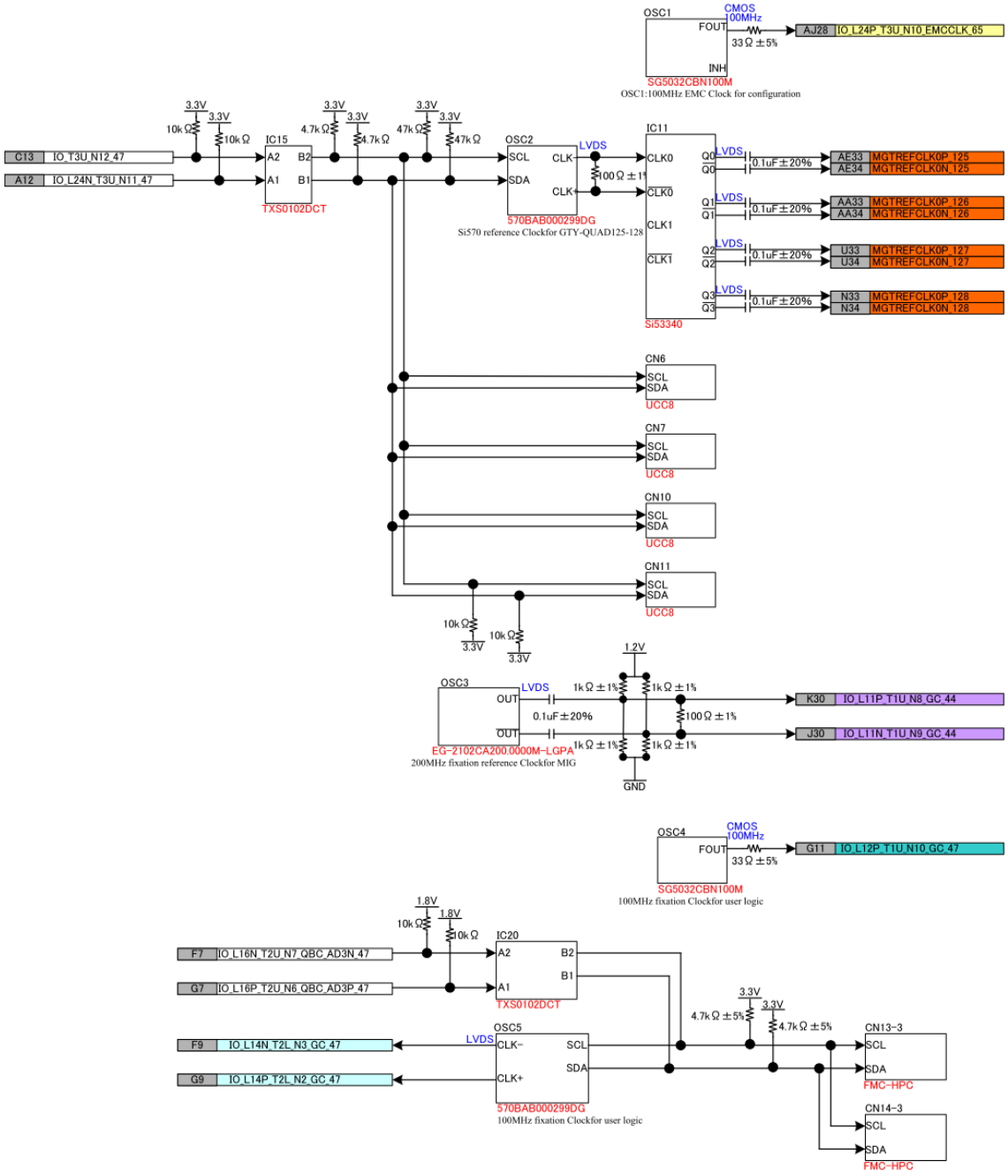

Figure 12 clock system diagram

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3.11. Power supply

・DCDC modules (Linear Technology).

And it can set output voltage and current limit etc from PC software.

・"Address" in the figure is the I2C address of DCDC that can be checked from the LTPowerPlay software.

I2C cannot connect from the FPGA.

・At the time of shipment, appropriate and minimum setting (output voltage, startup time, etc.) on this board is applied to each DCDC.

・DCDC setting project file for LTPowerPlay software is attached.

・When changing the setting of DCDC, short program J1 (for safety) and do the program.

・Also, during normal operation user can check the output state and temperature of the chip on the PC.

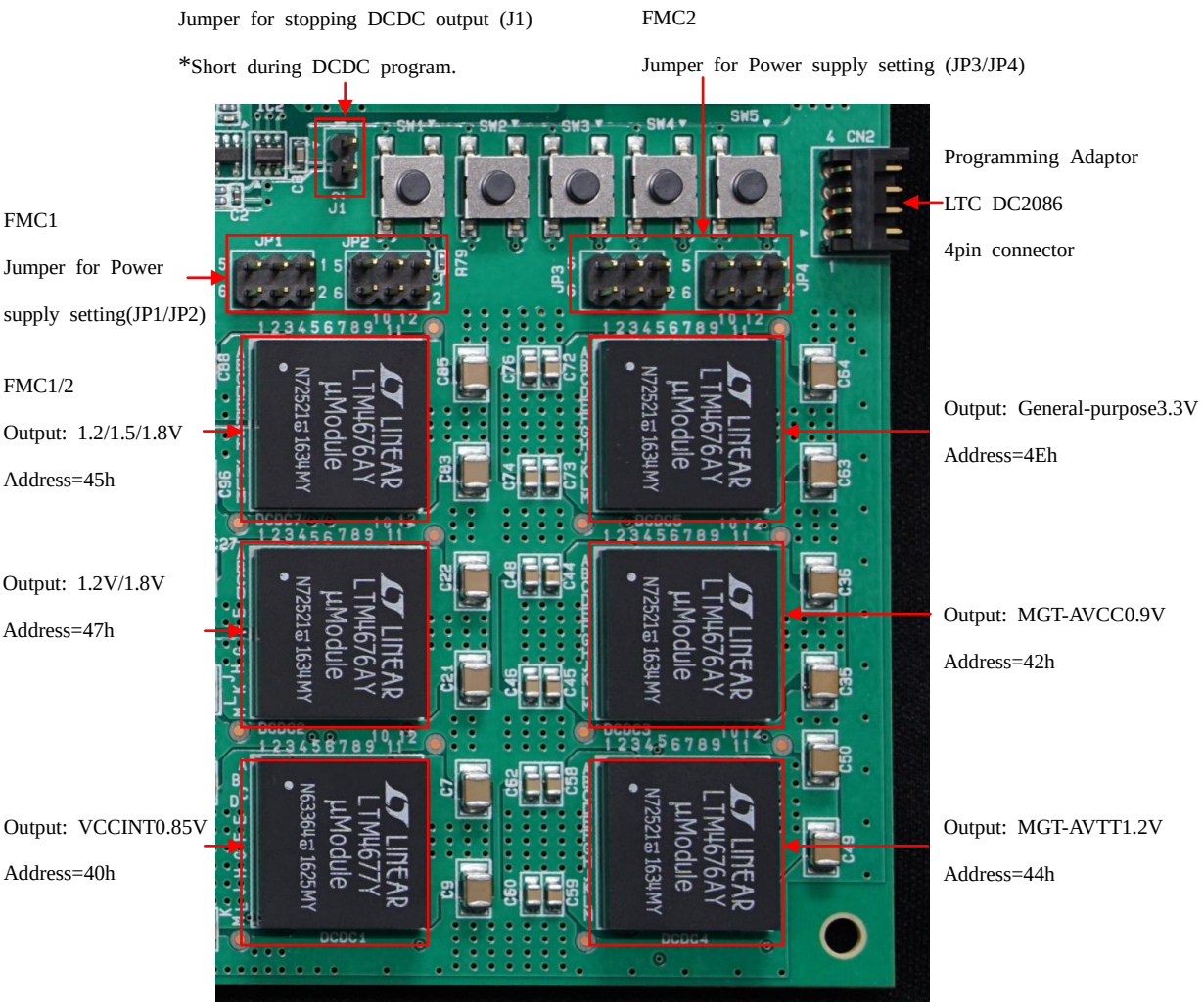

Figure 13 Power supply

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・The VADJ voltage setting of FMC1/2 becomes able to set it from an outside jumper not ROM data in DCDC.

・The output voltage is decided by the pair of the short position of JP1 and JP2, JP3 and JP4.

Table 6 FMC1 setting * The output is determined by combination (mV).

JP1 short position	JP2 short position	Output Voltage
1-2(1.7V)	1-2(+99mV)	1.8V (1.7+99mV)
3-4(1.5V)	3-4(+-0mV)	1.5V (1.5+0mV)
5-6(1.3V)	5-6(-99mV)	1.2V (1.3-99mV)

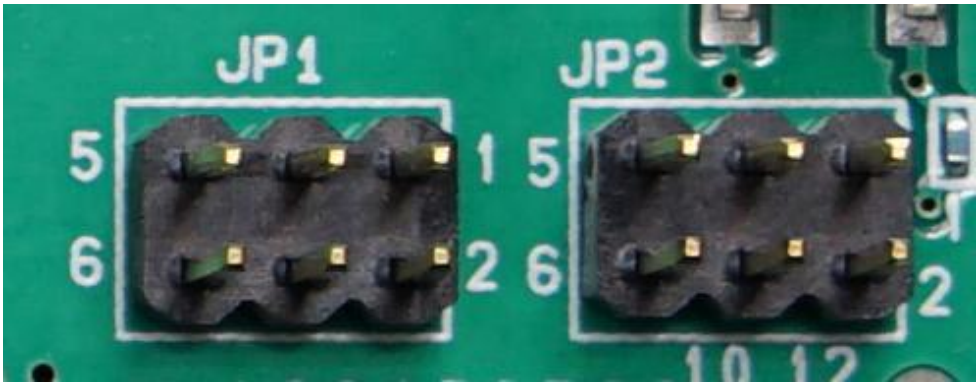

Figure 14 JP1 and JP2

Table 7 FMC2 setting * The output is determined by combination (mV).

JP3 short position	JP4 short position	Output Voltage
1-2(1.7V)	1-2(+99mA)	1.8V(1.7+99mV)
3-4(1.5V)	3-4(+-0mA)	1.5V(1.5+0mV)
5-6(1.3V)	5-6(-99mA)	1.3V(1.3-99mV)

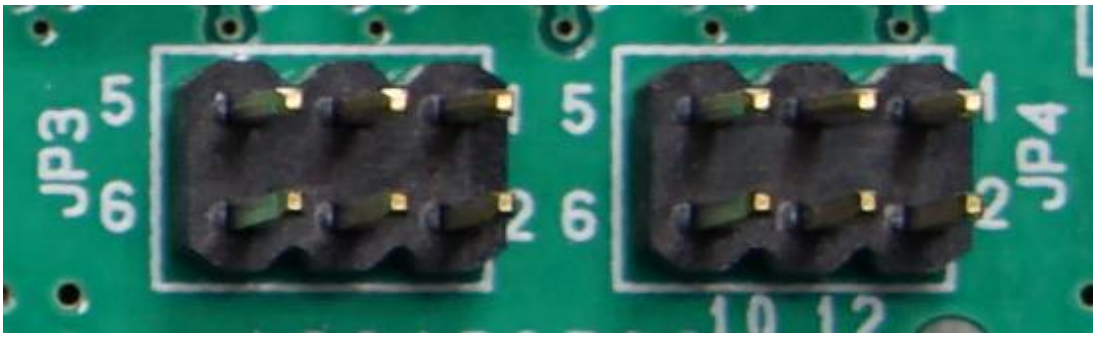

Figure 15 JP3 and JP4

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3.12. Power system diagram

The power supply system diagram of this board is shown below.

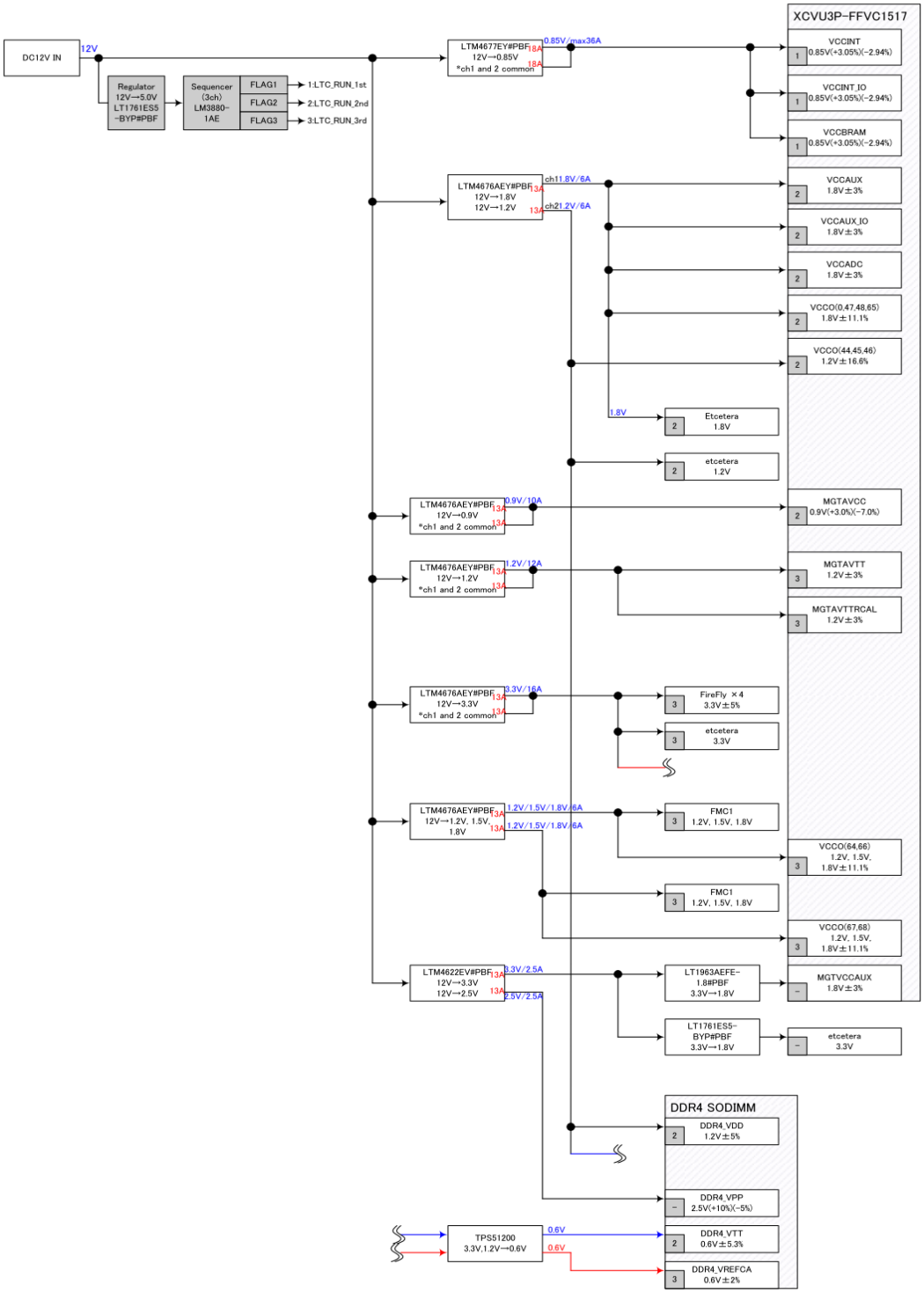

Figure 16 Power system diagram

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3.13. Miscellaneous

・An XDC file for pin location for VIVADO is attached.

・A sample design generated from IP catalog is attached.

→DDR4-2133 MIG Example Design

→PCIe x16 endpoint Example Design

→FireFly , GTY-iBERT Example Design for FMC1/2

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